

PHKD6N02LT

Dual TrenchMOS™ logic level FET

Rev. 02 — 12 August 2003

Product data

1. Description

Dual N-channel enhancement mode field-effect transistors in a plastic surface mount package using TrenchMOS™ technology.

Product availability:

PHKD6N02LT in SOT96-1 (SO8).

2. Features

- Low on-state resistance
- Logic level compatible
- Dual device
- Surface mount package.

3. Applications

- DC-to-DC converters
- Notebook computers
- Portable appliances
- Battery chargers.

4. Pinning information

Table 1: Pinning - SOT96-1 (SO8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	source1 (s1)	<p>Top view MBK187</p> <p>SOT96-1 (SO8)</p>	<p>MBK725</p>
2	gate1 (g1)		
3	source2 (s2)		
4	gate2 (g2)		
5, 6	drain2 (d2)		
7, 8	drain1 (d1)		



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$	[1] -	10.9	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	4.17	W
T_j	junction temperature		-	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 3\text{ A}$	16	20	mΩ
		$V_{GS} = 2.5\text{ V}; I_D = 3\text{ A}$	25	35	mΩ

[1] Single device conducting.

6. Ordering information

Table 3: Ordering information

Type number	Package		Version
	Name	Description	
PHKD6N02LT	SO8	Plastic small outline package; 8 leads	SOT96-1

7. Limiting values

Table 4: Limiting values

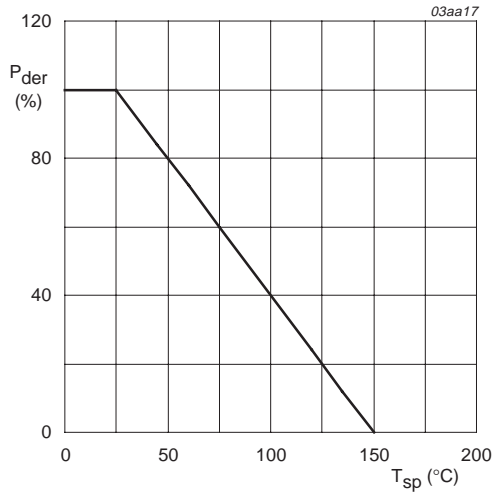
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25\text{ to }150\text{ °C}$	-	20	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25\text{ to }150\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage (DC)		-	±12	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}; \text{Figure 2 and 3}$	[1] -	10.9	A
		$T_{sp} = 100\text{ °C}; \text{Figure 2}$	[1] -	6.8	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}; t_p \leq 100\text{ }\mu\text{s}; \text{Figure 3}$	[1] -	44	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}; \text{Figure 1}$	-	4.17	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

Source-drain (reverse) diode

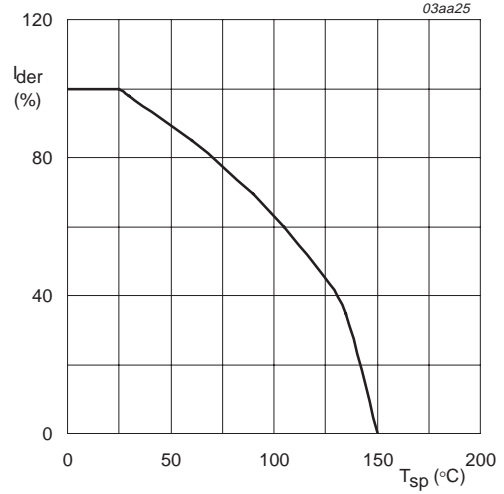
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	3.5	A
I_{SM}	peak (diode forward) source current	$T_{sp} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s}$	-	44	A

[1] Single device conducting.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

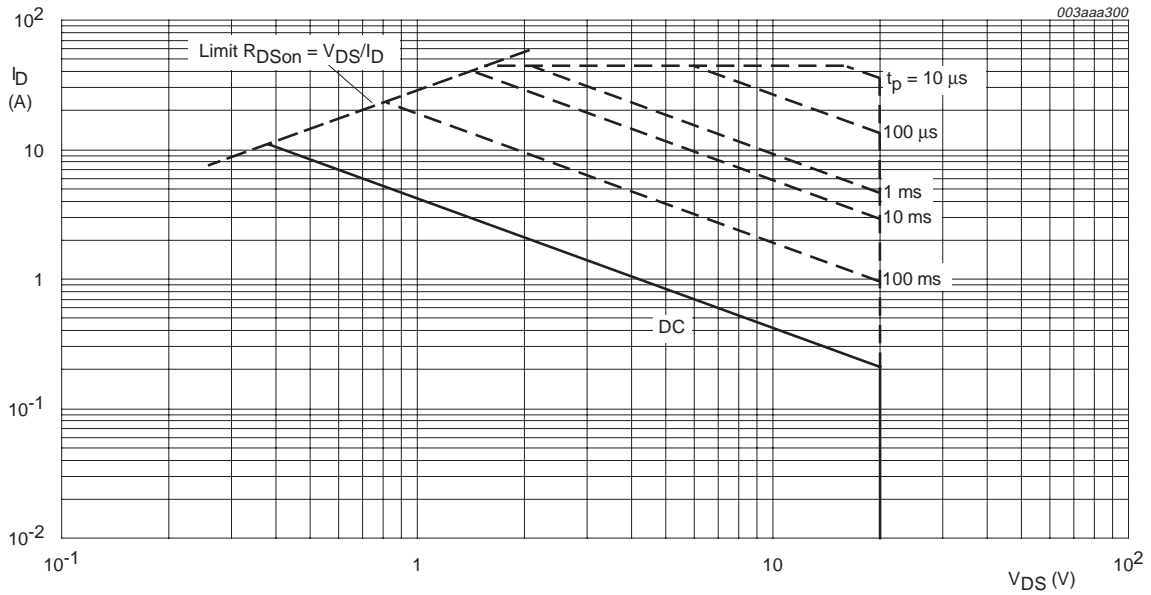
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 4.5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

8. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	30	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on printed-circuit board	-	70	-	K/W

8.1 Transient thermal impedance

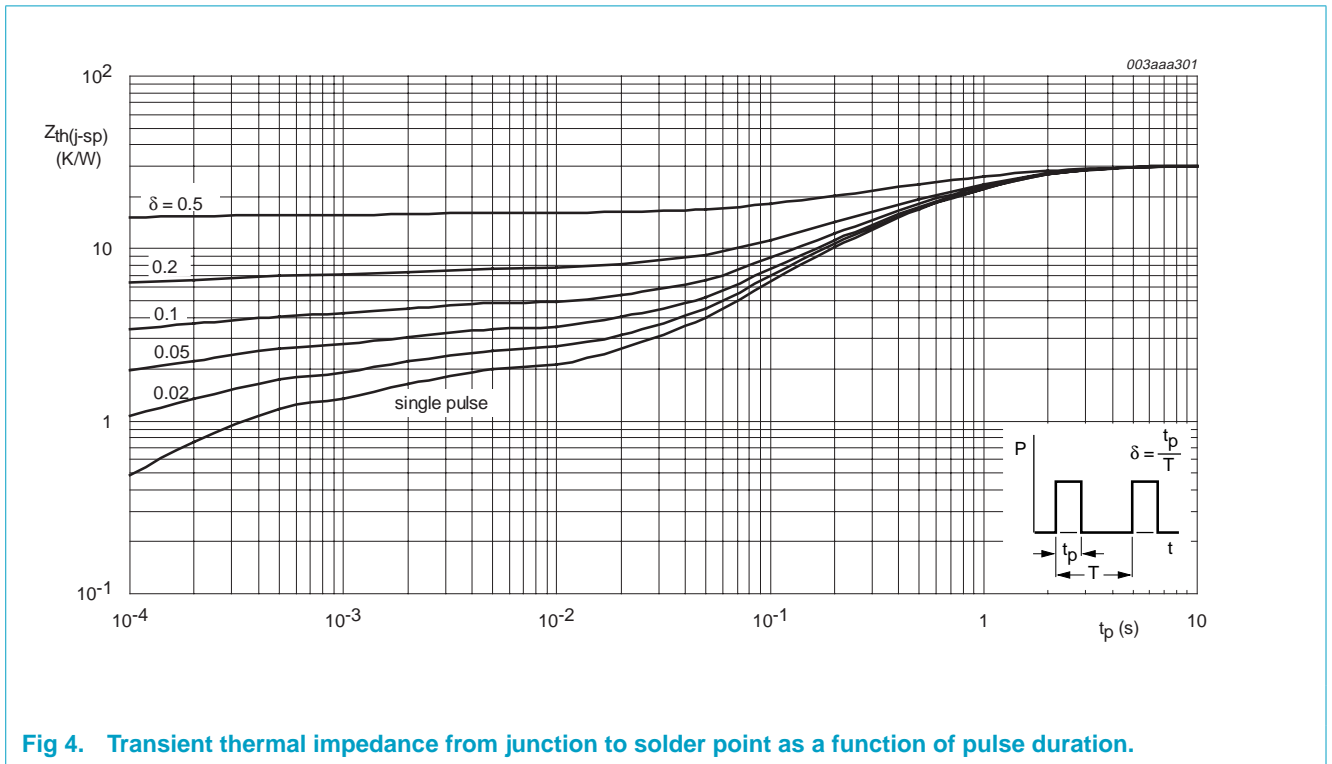
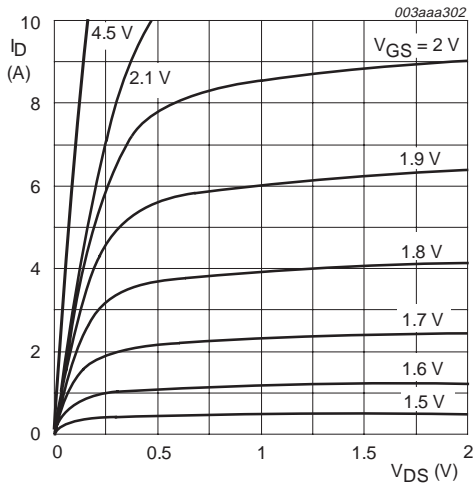


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

9. Characteristics

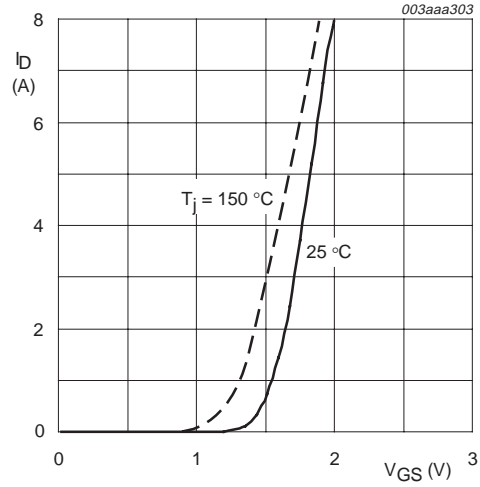
Table 6: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
Static characteristics								
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V	20	-	-	V		
V _{GS(th)}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = 10 V; Figure 9	0.5	-	1.5	V		
I _{DSS}	drain-source leakage current	V _{DS} = 20 V; V _{GS} = 0 V	-	T _j = 25 °C	0.05	10	μA	
				T _j = 150 °C	-	-	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±12 V; V _{DS} = 0 V	-	-	±100	nA		
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 3 A; Figure 7 and 8	-	T _j = 25 °C	16	20	mΩ	
				T _j = 150 °C	-	-	35	mΩ
				V _{GS} = 2.5 V; I _D = 3 A	25	35	mΩ	
Dynamic characteristics								
Q _{g(tot)}	total gate charge	I _D = 6 A; V _{DD} = 16 V; V _{GS} = 5 V; Figure 13	-	15.3	-	nC		
Q _{gs}	gate-source charge		-	2.2	-	nC		
Q _{gd}	gate-drain (Miller) charge		-	6	-	nC		
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DD} = 10 V; f = 1 MHz; Figure 11	-	950	-	pF		
C _{oss}	output capacitance		-	355	-	pF		
C _{rss}	reverse transfer capacitance		-	256	-	pF		
t _{d(on)}	turn-on delay time	V _{DS} = 10 V; R _D = 3.3 Ω; V _{GS} = 5 V; R _G = 4.7 Ω	-	15	-	ns		
t _r	rise time		-	49	-	ns		
t _{d(off)}	turn-off delay time		-	50	-	ns		
t _f	fall time		-	23	-	ns		
Source-drain (reverse) diode								
V _{SD}	source-drain (diode forward) voltage	I _S = 6 A; V _{GS} = 0 V; Figure 12	-	-	1.2	V		
t _{rr}	reverse recovery time	I _S = 6 A; dI _S /dt = -100 A/μs; V _R = 20 V;	-	40	-	ns		
Q _r	recovered charge	V _{GS} = 0 V	-	7	-	nC		



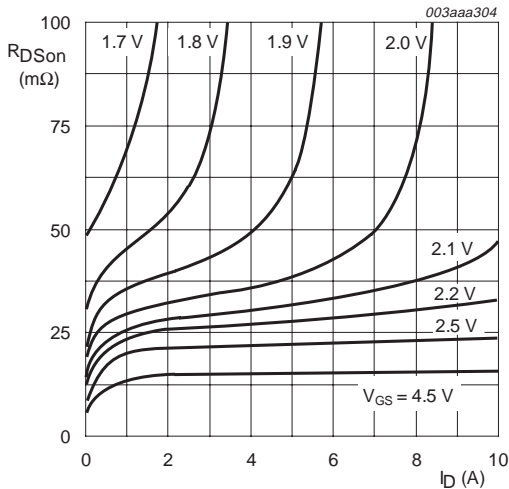
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



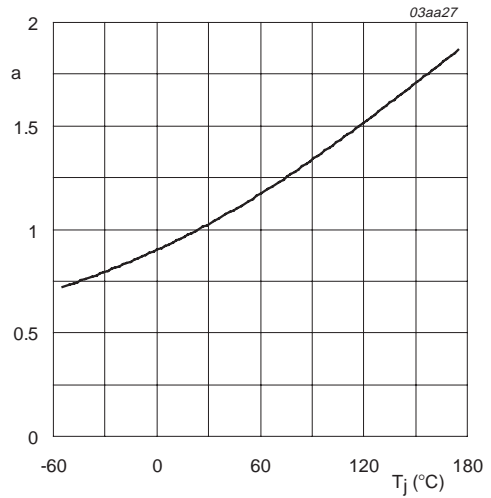
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



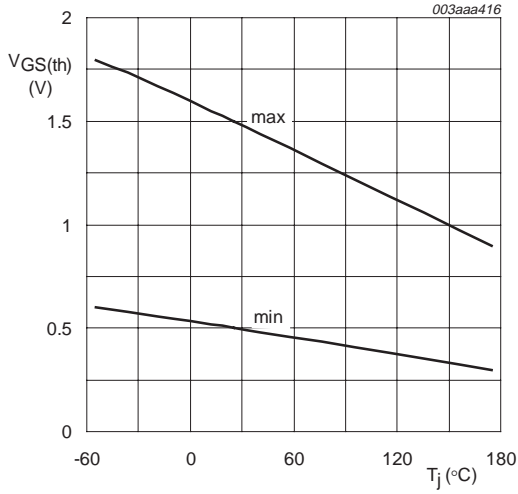
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



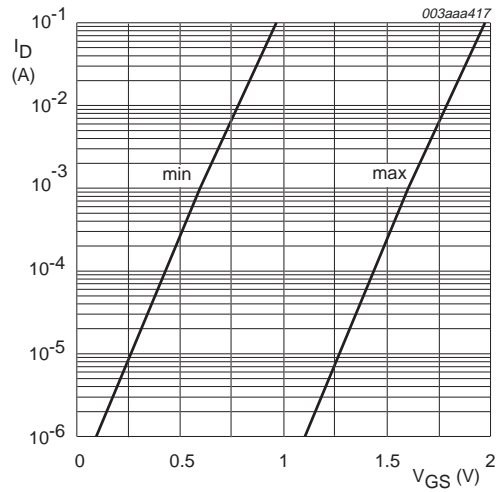
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



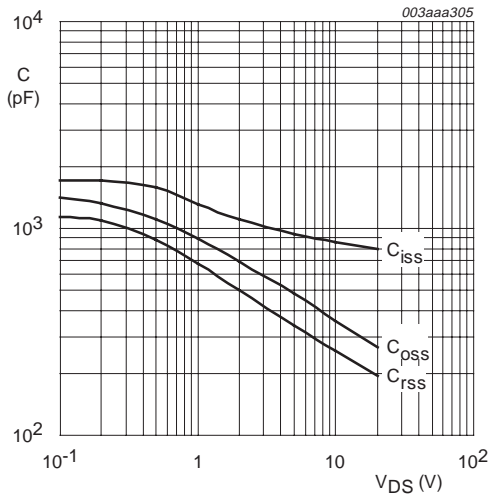
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



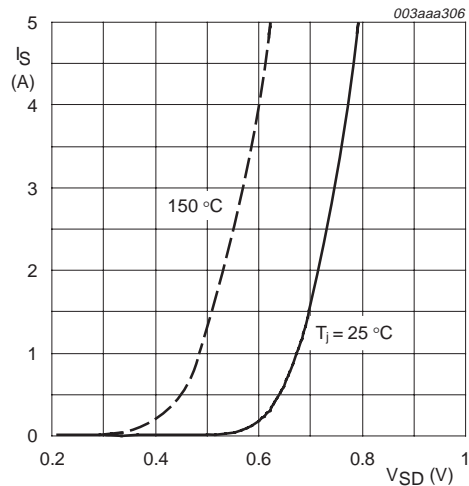
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



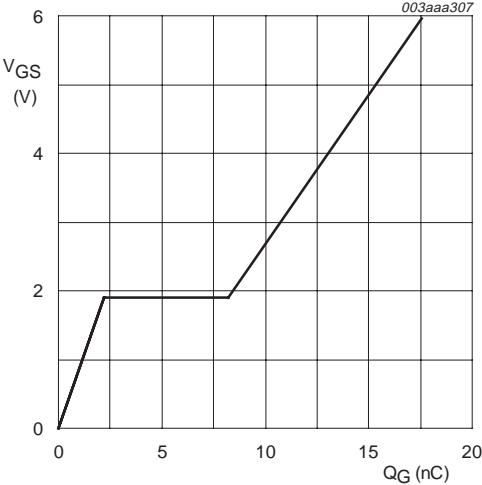
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25 \text{ °C and } 150 \text{ °C}; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 6\text{ A}; V_{DD} = 16\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

10. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

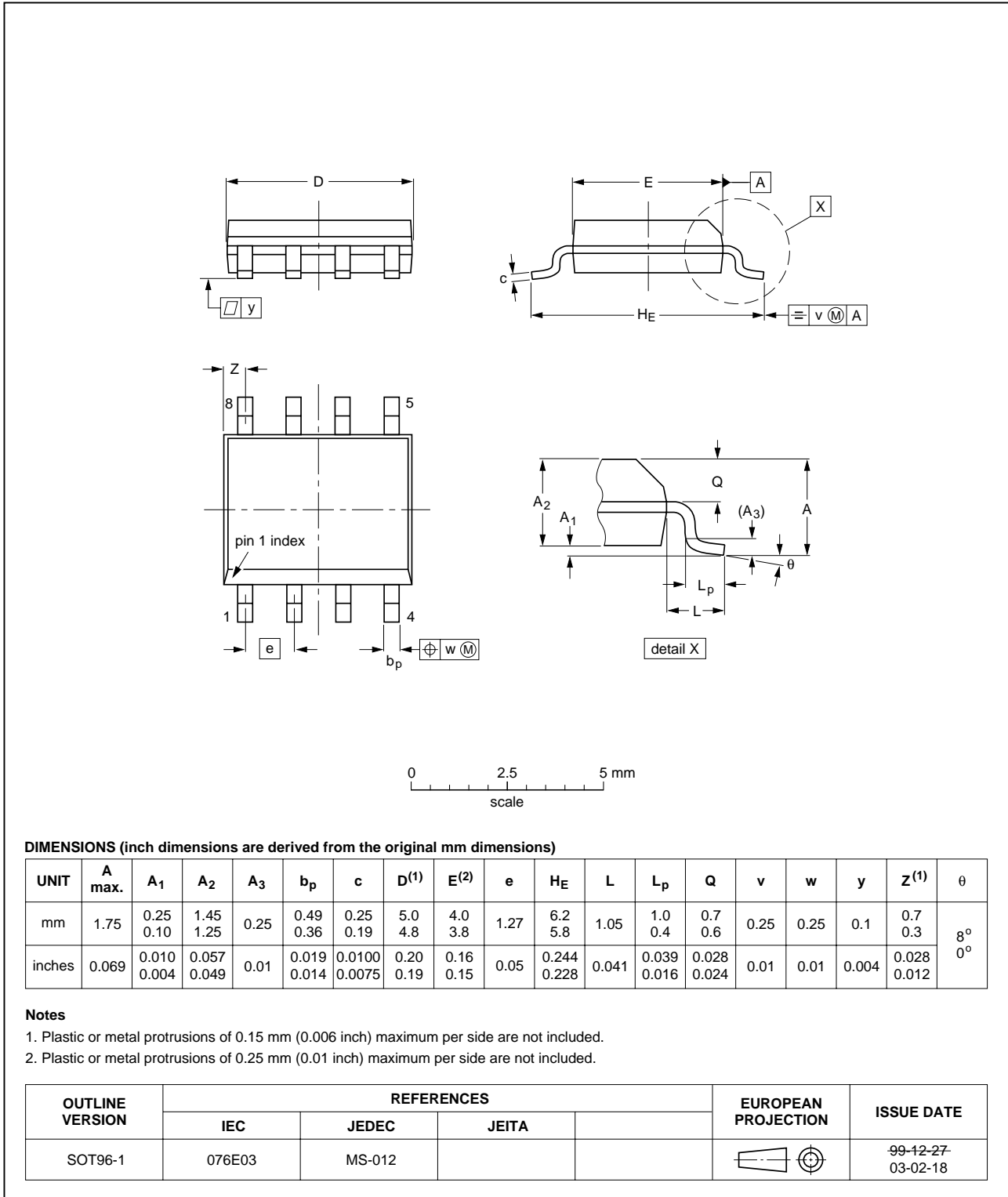


Fig 14. SOT96-1 (SO8).

11. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
02	20030812	200209008	Product data (9397 750 10688). Modifications: <ul style="list-style-type: none">• I_D data updated in Table 2 and 4.• P_{tot} data updated in Table 2 and 4.• R_{DSon} data updated in Table 2.• $R_{th(j-a)}$ data added in Table 5.• Characteristics updated in Table 6.• Figure 3, 5, 6, 7, 9, 10, 11, 12 and 13 updated.
01	20010907	-	Product data (9397 750 08522)

12. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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